

**IN THE CLAIMS:**

1           1.     (Previously Presented) A cache controller used in a computer system that  
2 includes a cache memory, a main memory, and a microprocessor which concurrently executes a  
3 plurality of tasks, comprising:

4                 a region managing unit operable to manage a plurality of regions in the cache  
5 memory in correspondence with the plurality of tasks;

6                 an address receiving unit operable to receive, from the microprocessor, an address  
7 of a location in the main memory at which data to be accessed to execute one of the plurality of  
8 tasks is stored;

9                 a judging unit operable to judge whether the data stored at the received address is  
10 stored in the cache memory, by searching all of the plurality of regions in the cache memory; and

11                a caching unit operable to acquire, if the judging unit judges that the data is not  
12 stored in the cache memory, a data block including the data from the main memory, and store the  
13 acquired data block into a region in the cache memory corresponding to the task.

1           2.     (Original) The cache controller of Claim 1,

2                 wherein the region managing unit divides the cache memory into the plurality of  
3 regions equal in number to the plurality of tasks, and manages the plurality of regions in a one-  
4 to-one correspondence with the plurality of tasks.

1           3.     (Original) The cache controller of Claim 2,

2                 wherein the region managing unit receives information about how many tasks are  
3 concurrently executed by the microprocessor and a size of memory required for execution of

4 each of the plurality of tasks, and divides the cache memory into the plurality of regions based on  
5 the received information.

1 4. (Original) The cache controller of Claim 3, further comprising:  
2 a task ID receiving unit operable to receive a task ID of the task,  
3 wherein the region managing unit manages the plurality of regions in a one-to-one  
4 correspondence with task IDs of the plurality of tasks, and  
5 the caching unit stores the acquired data block into the region in the cache  
6 memory corresponding to the received task ID.

1 5. (Original) The cache controller of Claim 4,  
2 wherein the task ID is an address of a location in the main memory at which the  
3 task is stored as a program.

1 6. (Original) The cache controller of Claim 4,  
2 wherein the task ID is generated by converting an address of a location in the  
3 main memory at which the task is stored as a program.

1 7. (Original) The cache controller of Claim 4,  
2 wherein the microprocessor performs multitasking under control of an operating  
3 system, and  
4 the task ID is a process ID assigned by the operating system.

1 8.-9. (Cancelled)

10. (Original) The cache controller of Claim 4,  
wherein the cache memory is made up of a plurality of ways, and  
the plurality of regions each contain at least one way.

11. (Cancelled)

12. (Original) The cache controller of Claim 1,  
wherein the region managing unit divides the cache memory into a specific region  
and a nonspecific region, and manages the specific region in correspondence with a specific task  
out of the plurality of tasks, and  
the caching unit stores the acquired data block into the specific region if the task  
is the specific task, and into the nonspecific region if the task is other than the specific task.

13. (Original) The cache controller of Claim 1,  
wherein the microprocessor concurrently executes a first task, a second task, and a  
third task,  
the region managing unit divides the cache memory into a first region and a  
second region, and manages the first region in correspondence with the first task and the second  
task, and the second region in correspondence with the third task, and  
the caching unit stores the acquired data block into the first region if the task is  
the first task or the second task, and into the second region if the task is the third task.

14. (Previously Presented) A cache control method used in a computer system that  
includes a cache memory, a main memory, and a microprocessor which concurrently executes a  
plurality of tasks, comprising:

4 a region managing step of managing a plurality of regions in the cache memory in  
5 correspondence with the plurality of tasks;

6 an address receiving step of receiving, from the microprocessor, an address of a  
7 location in the main memory at which data to be accessed to execute one of the plurality of tasks  
8 is stored;

9 a judging step of judging whether the data stored at the received address is stored  
10 in the cache memory, by searching all of the plurality of regions in the cache memory; and

11 a caching step of acquiring, if the data is not stored in the cache memory, a data  
12 block including the data from the main memory, and storing the acquired data block into a region  
13 in the cache memory corresponding to the task.

1 15. (Previously Presented) A computer system comprising a cache memory, a cache  
2 controller, a main memory, and a microprocessor which concurrently executes a plurality of  
3 tasks, the cache controller including:

4 a region managing unit operable to manage a plurality of regions in the cache  
5 memory in correspondence with the plurality of tasks;

6 an address receiving unit operable to receive, from the microprocessor, an address  
7 of a location in the main memory at which data to be accessed to execute one of the plurality of  
8 tasks is stored;

9 a judging unit operable to judge whether the data stored at the received address is  
10 stored in the cache memory, by searching all of the plurality of regions in the cache memory; and

11 a caching unit operable to acquire, if the judging unit judges that the data is not  
12 stored in the cache memory, a data block including the data from the main memory, and store the  
13 acquired data block into a region in the cache memory corresponding to the task.

1 16. (Original) The computer system of Claim 15, further comprising:

2 an address converting unit operable to receive from the microprocessor a logical  
3 address showing the address of the location in the main memory at which the data to be accessed  
4 is stored, convert the logical address to a physical address, and send the physical address to the  
5 address receiving unit,

6 wherein the cache controller further includes:

7 a data block managing unit operable to manage the data block stored in the cache  
8 memory by the caching unit, using the physical address.

1 17. (Original) The computer system of Claim 15,

2 wherein the address receiving unit receives from the microprocessor a logical  
3 address showing the address of the location in the main memory at which the data to be accessed  
4 is stored,

5 the cache controller further includes:

6 a data block managing unit operable to manage the data block stored in the cache  
7 memory by the caching unit, using the logical address, and

8 the computer system further comprises:

9 an address converting unit operable to convert the logical address output from the  
10 cache controller to a physical address, and send the physical address to the main memory.